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News Briefs

MAXIM REPORTS 42ND CONSECUTIVE QUARTER OF INCREASED REVENUES AND 40TH CONSECUTIVE QUARTER OF INCREASED EARNINGS

Maxim Integrated Products, Inc., reported record net revenues of $109 million for the third quarter of fiscal 1996 ending March 31, 1996, compared to $66.6 million for the same period a year ago. This represents a 63.6% increase in net revenues from the same quarter a year ago. Net income increased 237.6% to $34.2 million (or $0.48 per share) for the current quarter, compared to net income of $10.1 million (or $0.15 per share) for the same quarter in fiscal 1995. Operating income was a record 47.2% of net revenues, compared to 22.3% for Q395. Annualized return on equity increased to 53.9% for Q396, compared to 25.2% for fiscal 1995. During the quarter, the Company increased cash and short-term investments by $4.5 million after paying for over $23 million in property, plant, and equipment.

During the third quarter of fiscal 1996, the Company experienced strong demand for its advanced CMOS products that have been introduced over the past two years and for its communications products manufactured with the Company's state-of-the-art high-frequency processes. At the same time, the Company's end-market booking rates were flat with the prior quarter's levels. End-market bookings consist of orders on the Company from its OEM customers and orders received by the Company's distributors from their OEM customers. The Company's backlog shippable in the next 12 months declined $13 million to approximately $182 million, largely as a result of $28 million of order cancellations primarily from U.S. distributors.

Neither end-market bookings nor total net bookings on the Company are necessarily indicative of future revenue levels. The timing of orders by OEM customers fluctuates considerably, reflecting: (1) their internal development programs, (2) their manufacturing plans, and (3) lead times quoted by the Company. Additionally, the timing of orders and cancellations of orders by distributors is often dictated largely by their own balance sheet concerns, as well as their views on the availability of supply.

Jack Gifford, Chairman, President, and CEO, commented: "We are pleased that our manufacturing capacity has now risen to the point that, if we continue the progress we have been making, we should be able to meet the demand on 80% of our product lines by the end of the fourth quarter. As we enter fiscal 1997, we expect to continue to be manufacturing constrained on our advanced CMOS products that have been introduced over the past two years and our communications products manufactured on our state-of-the-art high-frequency processes. Together these products now account for approximately 20% of our current demand. We believe that we will be able to make significant progress on the manufacturing capacity issues related to these technologies over the next two quarters."

Mr. Gifford also noted: "Last summer we made estimates of end-market demand for fiscal 1996, attempting to separate out the effects of the sudden surge in orders experienced at that time, which was being exaggerated primarily by orders from U.S. distribution. Our prediction, at that time, of end-market demand for fiscal 1996 appears to have been relatively accurate."

Mr. Gifford commented further: "The results reported this quarter represent ten years of increased earnings, and over ten years of increased revenues over each prior quarter during that period. We are very proud that Maxim is the only company in the analog semiconductor industry today that can make this claim."

MAXIM DESIGN IDEAS WELL ACCEPTED WORLDWIDE

During calendar year 1995, Maxim strengthened its reputation for analog expertise by publishing 36 original design ideas in the US and the UK: 17 in *EDN*, 10 in *Electronic Design*, and 9 in British magazines. Of the 17 in *EDN*, 5 were voted "best of the issue."

Supervisor ICs monitor battery-powered equipment

*To ensure correct operation, most microprocessor-based systems require supervision during power-up and power-down, and when entering or exiting shutdown or sleep mode. The supervisor may only provide a power-on reset, or it may offer additional functions, such as backup-battery management, memory-write protection, low-line early warning, or a software watchdog (***Figure 1***).*

You can get these functions all together or in various combinations, by selecting one of the many available microprocessor (µP) supervisor ICs (also called power-on resets, power-good circuits, reset circuits, etc.). The following discussion helps you choose the one best suited to your application, and offers solutions for many common µP supervisory problems.

First, determine the V_{CC} threshold voltage for which resets will be issued. (The assertion of RESET blocks µP operation when the supply voltage is out of tolerance.) Typical power-on reset circuits consist of a voltage reference, comparator, and timer. Comparing the reference voltage with the rising V_{CC} (via a voltage divider) enables the comparator to make an output transition when V_{CC} crosses a threshold (V_{RST}) set by the divider. This transition triggers the timer, which maintains the reset as necessary to prevent software execution until the system oscillator has started and stabilized.

When V_{CC} falls below V_{RST}, the supervisor again issues a reset and maintains it as long as V_{CC} remains below V_{RST}. For some microcontrollers (µCs), a simple RC circuit is recommended for timing this power-on reset; others provide reset circuitry on the µC chip. Those approaches, however, assume the supply-voltage behavior is predictable. They don't protect against the code-execution errors that can occur as a result of power-down, or more importantly, during "brownouts," in which V_{CC} can fall slightly out of regulation for an extended period. Supervisory ICs are most valuable for these power-down and brownout conditions.

Factors that affect the threshold value include the tolerance on V_{CC}, the minimum and maximum supply voltages allowed for the system ICs, and the possible need to specify the design for worst-case combinations of these variables. For many systems, the reset function is not intended to cover all possible conditions including the worst-case combinations over temperature. A system might include ICs specified only to 4.75V minimum, for example, yet depend on a supervisor whose min/max trip threshold is 4.5V/4.75V. In that case, the supervisor asserts a reset only after V_{CC} has fallen below the minimum voltage guaranteed for IC operation.

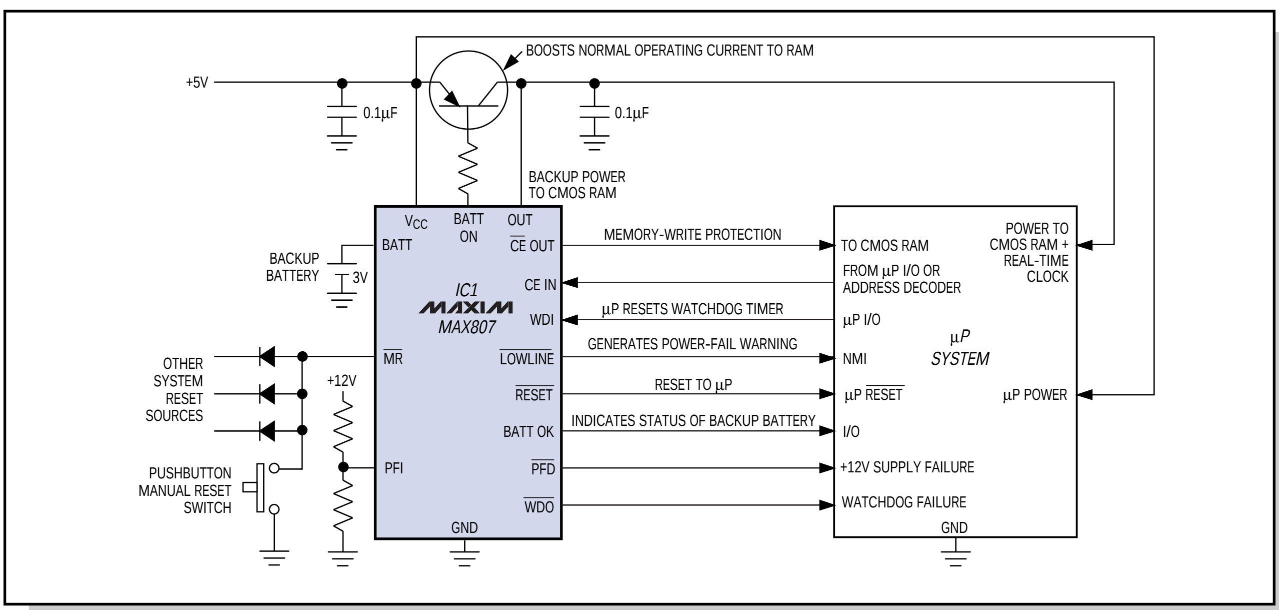


Figure 1. A feature-laden µP supervisor (IC1), with the help of the µP itself, performs a variety of functions in this typical application circuit.

The alternative is to choose a reset threshold between 4.75V and (perhaps) 4.85V. However, these values might allow resets to occur before they are needed. In general, you must decide whether you can tolerate a lower threshold, in order to gain operating time at lower voltages; or whether the extra expense and reduced operating time associated with a higher threshold are a fair trade for the benefit of tighter accuracy. Supervisor ICs are now available with reset-threshold tolerances as tight as ±1% (**Figure 2**).

Monitor more than one supply

Many applications require both 5V and 3.3V supplies, and if either loses regulation, you must typically reset the whole system. You also need an appropriate duration of power-on reset to ensure proper operation during power-up. A supervisory IC with a power-fail comparator and a manual reset input ($\overline{\text{MR}}$) offers a cost-effective solution to these problems.

If you choose a supervisory IC whose internal threshold is set to monitor 3.3V, you can then use the uncommitted power-fail comparator to monitor the 5V supply: simply route the power-fail-comparator output (PFO) back to the $\overline{\text{MR}}$ input (**Figure 3**). These connections cause the IC to assert $\overline{\text{RESET}}$ when either supply loses regulation. The IC is powered from 3.3V, so the $\overline{\text{RESET}}$ output swings 3.3V when active. That level satisfies the V_{IH} requirement of most 5V processors, so the $\overline{\text{RESET}}$ output can usually drive both 3V and 5V processors. If necessary, you can route other system-reset signals to the $\overline{\text{MR}}$ input with diode-OR connections. (Even without these connections a diode is required from the $\overline{\text{MR}}$ input to the PFO output.)

Early warning for shutdown routine

Critical systems often require an early warning when the power-supply voltage (V_{CC}) begins to fall. The warning allows time for the µP to store vital data and perform "housekeeping" chores before the declining V_{CC} causes the supervisor to issue a hard reset. If the raw dc input voltage is accessible, it can be monitored with an under-voltage or power-fail comparator, which in turn asserts a processor interrupt to indicate when the unregulated supply is collapsing.

If you don't have access to this raw input voltage, you must generate the early-warning and reset signals while monitoring the same regulated supply. You can use a single threshold detector for the low-line signal plus a delay timer for the reset signal, or use two different

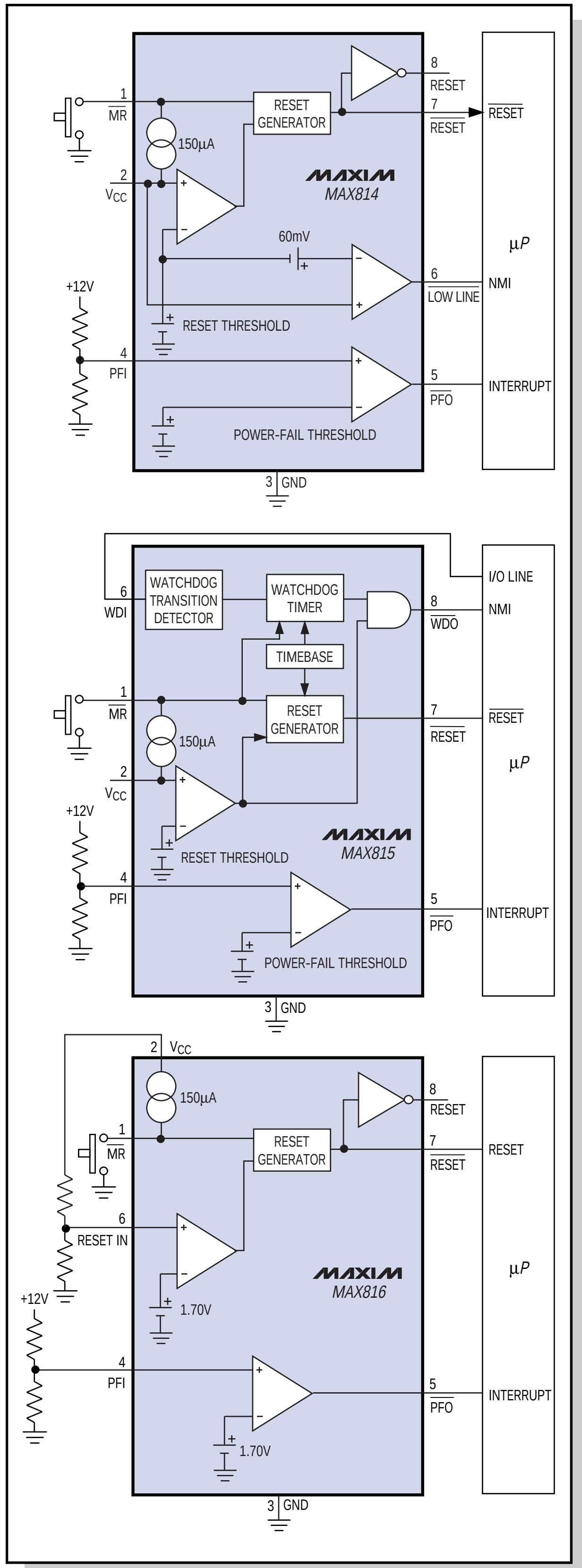


Figure 2. These three ICs offer different combinations of supervisory functions, but each monitors V_{CC} with ±1% accuracy.

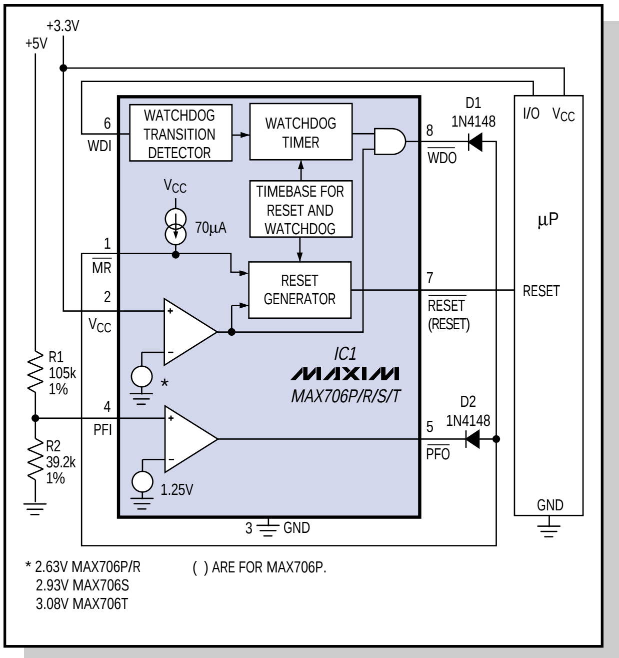


Figure 3. Configured as shown, this supervisory IC monitors both 3.3V and 5V supplies.

comparators—one for $t_{LOWLINE}$ and one for t_{RST}. Either way, you must ensure that V_{CC} remains valid long enough to complete the shutdown routine that follows an interrupt from the low-line signal.

The time required to complete a shutdown/backup routine varies widely with the application, as does the fall rate of V_{CC}. Thus, you must adjust the delay from low-line to reset according to the application. The two-threshold approach is more flexible than the time-delayed-reset approach. By adjusting the low-line threshold tens of millivolts above the reset threshold and adjusting the V_{CC} fall rate to comply with time requirements for the shutdown routine, you can make one IC serve many different applications.

In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine during the interval between the low-line warning and reset. If the V_{CC} fall time is rapid, as when a high-side switch is opened during normal operation, add capacitance on the load side of the switch to slow the decline of V_{CC} and provide time for executing the shutdown routine. In MAX814 supervisors, for example, the power-fail comparator's delay (less than 50µs) may or may not affect your application.

First, calculate the worst-case time required for the shutdown routine. Using this value, the worst-case load current, and the minimum low-line to reset-threshold difference ($V_{LR(min)}$), calculate the capacitance necessary for completion of the shutdown routine before reset occurs:

$$C_{HOLD} > I_{LOAD} \frac{t_{SHDN}}{V_{LR(min)}}$$

where I_{LOAD} is the current being drained from the capacitor, $V_{LR(min)}$ is the minimum difference between the low-line and reset thresholds, and t_{SHDN} is the time required for an orderly shutdown to occur, including the reset comparator's propagation delay.

Placing the low-line threshold above the reset threshold can allow false low-line triggers due to noise. To overcome this problem, filter the noise with adequate bypassing, and use software to monitor the low-line interrupt after the shutdown routine is completed. When the processor receives an interrupt from the low-line comparator, it completes the backup/shutdown routine and then returns to monitor the interrupt. If a line or load transient causes low-line to return high relatively quickly, the software initiates a "warm" start-up by reloading the stored parameters. If a power failure occurs, the low-line signal is followed by a reset signal, and the normal battery-backup mode of operation begins.

DC-DC boost circuit extends shutdown time

If a backup/shutdown routine requires more time than you can reasonably provide with storage capacitors, you can use a dc-dc converter to sustain V_{CC} while the shutdown routine is in progress. The µP can then shut down the dc-dc converter once the backup is complete.

In **Figure 4**, for example, IC2 is a step-up converter that provides 5V to the system and µP supervisor (IC3) when the main 5V supply fails. At the onset of such a power failure, as the main supply falls below 4.65V, IC1 turns off Q1, brings IC2 out of shutdown, and interrupts the µP. IC2 then boosts the supply voltage from 4.65V back to 5V. The reset threshold is not encountered, so a reset to the µP is not issued. When the µP finishes its shutdown routine, it simply pulls IC2 into shutdown again and the system goes into its normal battery-backup mode.

The boost converter delivers up to 100mA while powered from a lithium cell that has been drained to 2.5V. If desired, you can provide separate batteries for the RAM backup and the boost converters.

Guarding against false resets

The supervisory circuit must not issue resets in response to system noise or V_{CC} load transients. About 50mV of

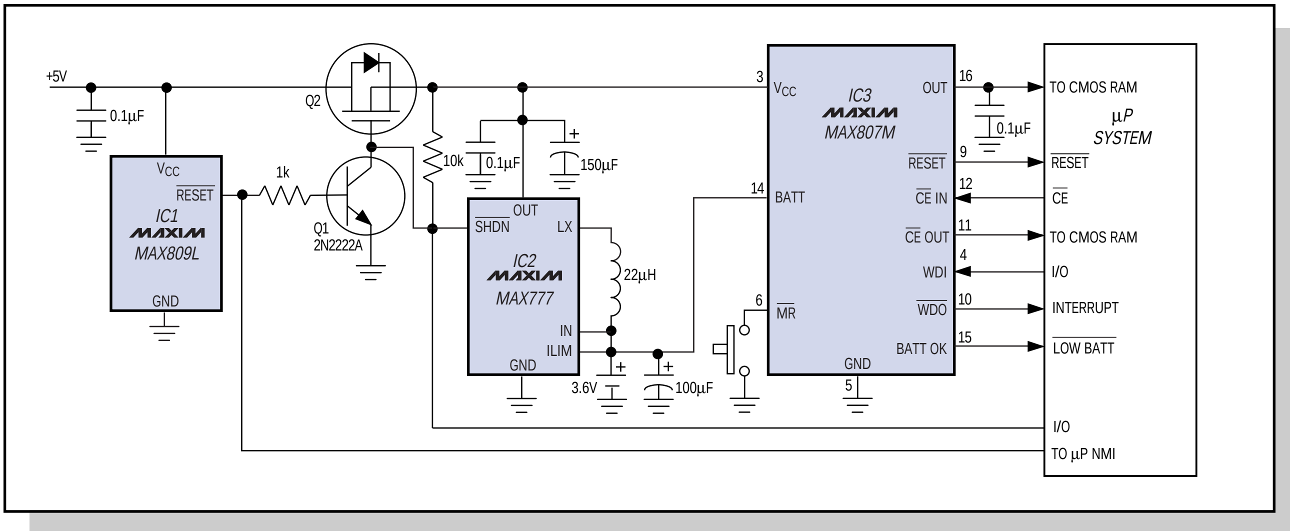


Figure 4. A threat of V_{CC} loss causes the boost converter (IC3) to turn on and restore V_{CC} to its nominal level.

noise on the digital power-supply lines is common. Load transients, which occur when modules, peripherals, and other subsystems are turned on or off, can cause serious problems if the reset comparator's propagation delay is too short.

You can avoid false resets by choosing a supervisory circuit whose reset comparator has a propagation delay of 10µs to 30µs. Shorter propagation delays (of a few hundred nanoseconds) react quickly to V_{CC} transients, and are therefore likely to generate false resets. Long delays, on the other hand, can allow V_{CC} to fall too far outside the system IC's operating range before the processor is reset. The majority of 5V applications include sufficient capacitance to reduce the V_{CC} fall rate such that a reset occurs *before* V_{CC} falls below the minimum level specified in the IC's electrical characteristics.

Battery backup

For critical systems that require non-volatile memory, the designer can choose either erasable/programmable memory or a CMOS RAM with backup battery. EEPROMs and flash memory are rated not only for memory capacity, but also for the number of write cycles they can undergo. The most common non-volatile memory includes a switch that connects the CMOS RAM to the lithium backup battery or V_{CC}, whichever is higher.

Large capacitors (around 0.5F) offer a popular method for providing a short-duration memory backup. Called SuperCaps™ or MaxCaps™, these capacitors charge from V_{CC} through a diode during normal operation (**Figure 5**). Charging current is limited by the capacitors' internal series resistance, which is relatively high. The RAM is switched from V_{CC} to the capacitor when V_{CC} collapses below the IC's reset threshold. The available backup time depends on the level of quiescent current into the RAM and supervisor IC, and the self-discharge leakage of the capacitor itself. For the many systems that draw only tens of microamps in backup mode, such backup capacitors can maintain the memory contents for several hours. The 1µA quiescent currents of Maxim supervisors, for instance, are generally insignificant.

Backup-battery switchover in 3V applications presents a challenge: How do you determine when to switch between a 3.3V V_{CC} and a 3.6V lithium backup cell?

SuperCap is a trademark of Baknor Industries.
MaxCap is a trademark of The Carborundum Corp.

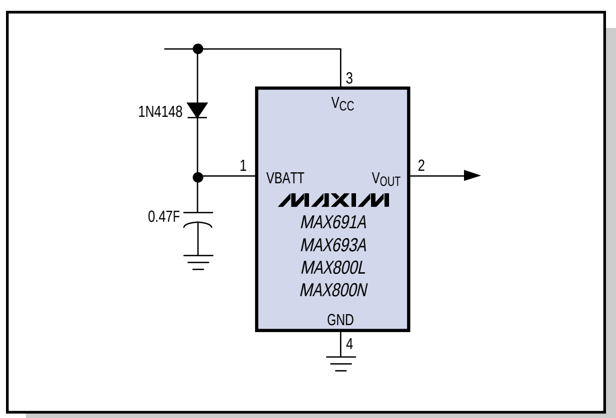


Figure 5. A very large capacitor (0.47F in this case) can serve as a backup battery in systems with low quiescent current.

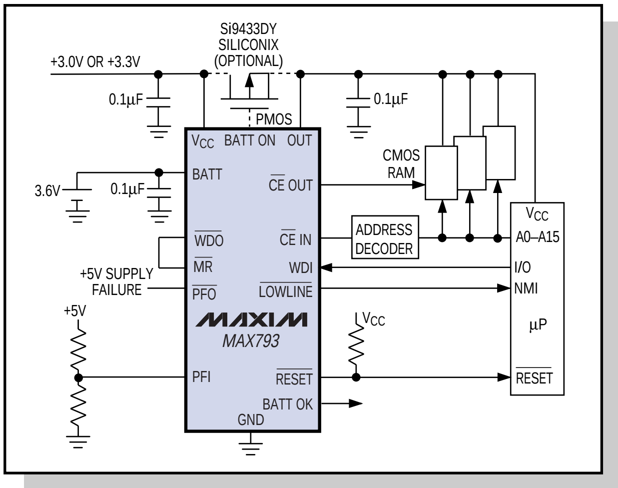


Figure 6. When V_{CC} sinks to slightly above 2V, this system switches the CMOS RAM from V_{CC} to the backup battery.

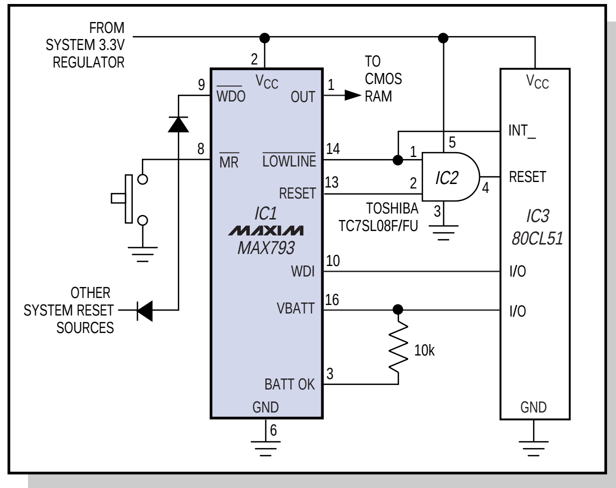


Figure 7. The AND gate preserves battery energy by preventing an unnecessary shift in microcontroller operation—from sleep mode to the higher-current idle mode.

One way is to define a ground-referenced voltage that is higher than the CMOS RAM's minimum standby voltage. Thus, V_{CC} supplies the RAM until it falls to slightly more than 2V; RAM is then switched to the backup battery (**Figure 6**).

Special cases

To conserve battery energy, designers of battery-operated portable equipment often make use of the 80CL51 µC's power-down mode. If the preservation of CMOS memory content is critical, IC1's $\overline{\text{LOWLINE}}$ output (Figure 6) generates an interrupt. This interrupt signal can trigger a shutdown routine when the main battery voltage goes low enough to cause V_{CC} to fall out of tolerance. RAM contents are kept alive by whatever energy remains in the battery.

With the µC in power-down mode and the supervisor's RESET connected directly to the µC's RST terminal, a V_{CC} decline below the reset threshold will cause RESET to go high. This, in turn, wakes up the µC and places it in run mode, increasing its quiescent current from approximately 100µA to 6mA. Battery voltage continues to fall and V_{CC} remains below the threshold, so 6mA will drain the battery, considerably shortening the available backup time.

Simply combining $\overline{\text{LOWLINE}}$ and RESET with an AND gate (**Figure 7**) ensures that IC3's RST is driven high only for the reset timeout period (not when V_{CC} is falling). In other words, RST goes high after V_{CC} has been restored (by recharging the battery or installing a fresh one) and has recrossed the low-line threshold. The AND gate thus allows the sleeping controller to remain in a sleep state.

With V_{CC} in its normal operating range, RESET is low and $\overline{\text{LOWLINE}}$ is high. When V_{CC} falls below the low-line threshold (typically 45mV above the reset threshold), $\overline{\text{LOWLINE}}$ goes low, signaling the 80CL51 to begin its shutdown routine. RESET asserts when V_{CC} encounters the reset threshold, but $\overline{\text{LOWLINE}}$ forces the AND-gate output to remain low.

On power-up $\overline{\text{LOWLINE}}$ remains low, therefore RST remains low until V_{CC} crosses the low-line threshold. RESET then propagates through to the RST terminal for the duration of the reset timeout period. As a result, the 80CL51 exits its sleep mode only when V_{CC} is valid.

Also desirable in this application is an ability to detect whether the battery has discharged below the safe RAM-backup voltage at any time during the sleep period. Using this information, the system decides whether to perform a "warm boot" based on the contents of the RAM, or a "cold boot" that starts from scratch because low battery voltage may have corrupted the RAM data. IC1's BATT terminal (pin 16) tells the µC which boot is appropriate.

IC1 has a low-battery comparator that normally indicates the state of a backup battery connected to its BATT terminal. This comparator output (BATT OK) is not latched. The application of Figure 7 has no backup battery, so you can use BATT to latch the state of BATT OK. Simply connect BATT to an available I/O pin on the 80CL51, and to the BATT OK terminal via a 10kΩ resistor.

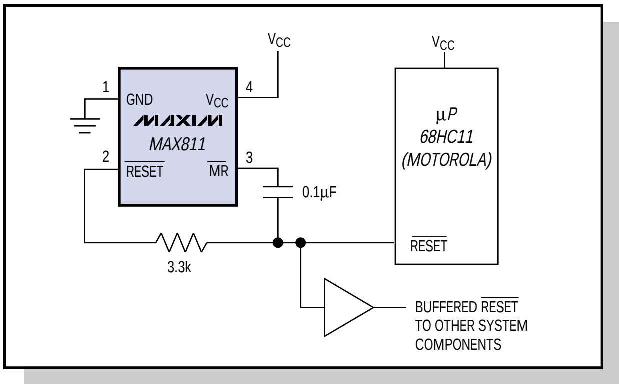


Figure 8. These connections allow dual control of the buffered reset line, and extend the duration of resets issued by the µP.

To set up for normal operation, the µC pulses the I/O line high for about 30µs, then configures the line as a high-impedance input. The comparator in IC1 drives BATT OK high, which pulls BATT high and latches it in that condition. The comparator is powered by V_{CC}, so its output in the high state is near V_{CC}. If V_{CC} goes as low as 2.25V at any time during the sleep period, the comparator output snaps low and pulls BATT low, latching it in the low condition. After V_{CC} is restored (by recharging the main battery or replacing it) the µC polls BATT before proceeding: high indicates a warm boot, and low indicates a cold boot.

µCs such as the Motorola 68HC11 have bidirectional reset pins that may contend with $\overline{\text{RESET}}$ from the supervisory IC. If the supervisor reset is high, for instance, and the µC tries to pull it low, the result may be an indeterminate logic level. **Figure 8** connections allow both the supervisor and µC to assert valid resets to the system, and also ensure sufficient duration for the reset pulses (µC resets may be too short for some devices in the system).

The capacitor enables resets from the supervisor and µC to pull $\overline{\text{MR}}$ low. $\overline{\text{MR}}$ going low initiates a 200ms timeout within the supervisor, producing a 200ms minimum pulse at its $\overline{\text{RESET}}$ terminal (pin 2) that overrides the µC $\overline{\text{RESET}}$ and drives the system reset line via the buffer. $\overline{\text{MR}}$ returns high as the capacitor charges. When the µC $\overline{\text{RESET}}$ de-asserts following the timeout delay, the capacitor discharges through the $\overline{\text{MR}}$ pull-up resistor and an internal ESD-protection diode.

(Circle 1)

Memory-backup supply is simple and efficient

The high-efficiency RAM-backup power supply of **Figure 1** delivers 5V at 1mA for inputs in the range 8V to 32V. Most single-chip regulators that operate over this range are bipolar ICs with quiescent currents comparable to the 1mA load current. This circuit, however, draws only 10µA when operating.

The JFET series-pass element operates as a switched current source in a switched linear regulator: at start-up, C1 is fully discharged and Q1 acts as a current source. V_{OUT} rises linearly as C1 charges, activating IC1 at 2V and continuing toward the 5V threshold set by R3 and R4. IC1 combines a CMOS micropower comparator and 1.182V bandgap reference. As V_{OUT} reaches its threshold, the comparator output goes low, turning off Q1 by reverse-biasing its gate-source junction. As the load current discharges C1 below the output threshold, Q1 turns back on and completes one switching cycle.

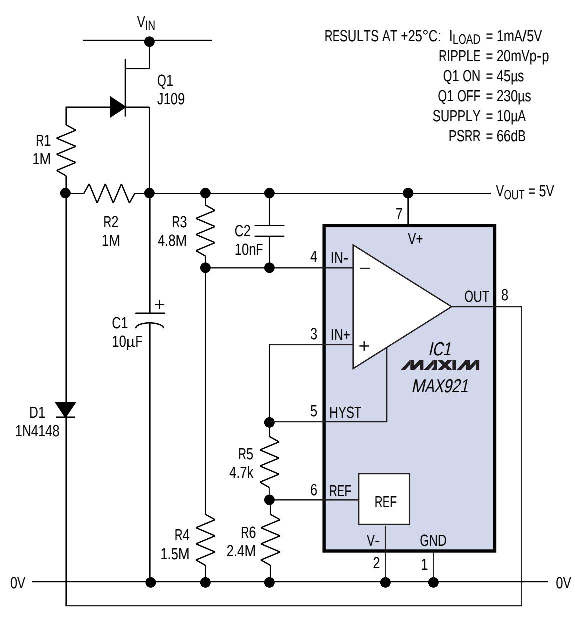


Figure 1. This simple RAM-backup power supply offers efficiency and versatility.

Q1's depletion characteristic ensures start-up for the circuit. It also ensures excellent PSRR (>60dB for $5.5V \leq V_{IN} \leq 30V$), because both the reference and the error amplifier receive power from the regulated output voltage. Q1 should be chosen for I_{DSS}, $V_{GS(OFF)}$, and V_{DS}. I_{DSS} is the current drawn at start-up, when Q1 is saturated (i.e., when V_{GS} is zero and $V_{DS} \geq V_{GS(OFF)}$). $V_{GS(OFF)}$, which determines the minimum allowed V_{IN}-V_{OUT} difference for proper circuit operation, must be less than V_{OUT} to ensure that Q1 can turn off. The Q1 device shown in the prototype circuit (J109) specifies a minimum I_{DSS} of 40mA, a $V_{GS(OFF)}$ between -6V and -2V, and a minimum V_{DS} of 25V. For production, a J113 type is more appropriate.

C2 reduces output ripple by speeding the propagation of feedback to the comparator's inverting input. Without C2, the high value of R3 (necessary to minimize the circuit's quiescent current) combines with parasitic capacitance to slow the regulator's response. The value shown (10nF) lowers the sawtooth-ripple voltage from $200mV_{p-p}$ to $20mV_{p-p}$. Larger C1 values further decrease the ripple while increasing the circuit's off time, which also reduces the average supply current. R1 and R2 determine the on time. R1 also limits the turn-off spikes produced by rapid high-to-low transitions on the gate of Q1.

IC1's pin 5 (HYST) lets the user add comparator hysteresis, adjustable via R5 and R6. The R6 value shown (2.4MΩ) makes the hysteresis value in mV (about 5mV in this case) numerically equal to the R5 value in kΩ.

A related idea appeared in the 10/2/95 issue of Electronic Design.

(Circle 2)

DESIGN SHOWCASE

Battery charger delivers 2.5A with >96% efficiency

Battery chargers are usually designed without regard for efficiency, but the heat generated by low-efficiency chargers can present a problem. For those applications, the charger of **Figure 1** delivers 2.5A with efficiency as high as 96%. It can charge a battery of one to six cells while operating from a car battery.

IC1 is a buck-mode switching regulator that controls the external power switch, Q1, and the synchronous rectifier, Q2. These n-channel MOSFETs are more efficient than equivalent p-channel types because their on-resistance is lower; therefore they drop less voltage when conducting a given amount of current. IC1 includes a charge pump for generating the positive gate-drive voltage required by Q1.

The battery-charging current develops a voltage across the 25mΩ resistor R3 that is amplified by the op amp and presented as positive-voltage feedback to IC1. This feedback enables the chip to maintain the charging current at 2.5A. While charging, the circuit can also supply current to a separate load, up to a limit set by the current-sense transformer, T1, and sense resistor, R1.

T1 improves efficiency by lowering power dissipation in R1. The transformer turns ratio (1:70) routes only 1/70 of the total battery-plus-load current through R1, creating a feedback voltage that enables IC1 to limit the overall current to a level compatible with the external components.

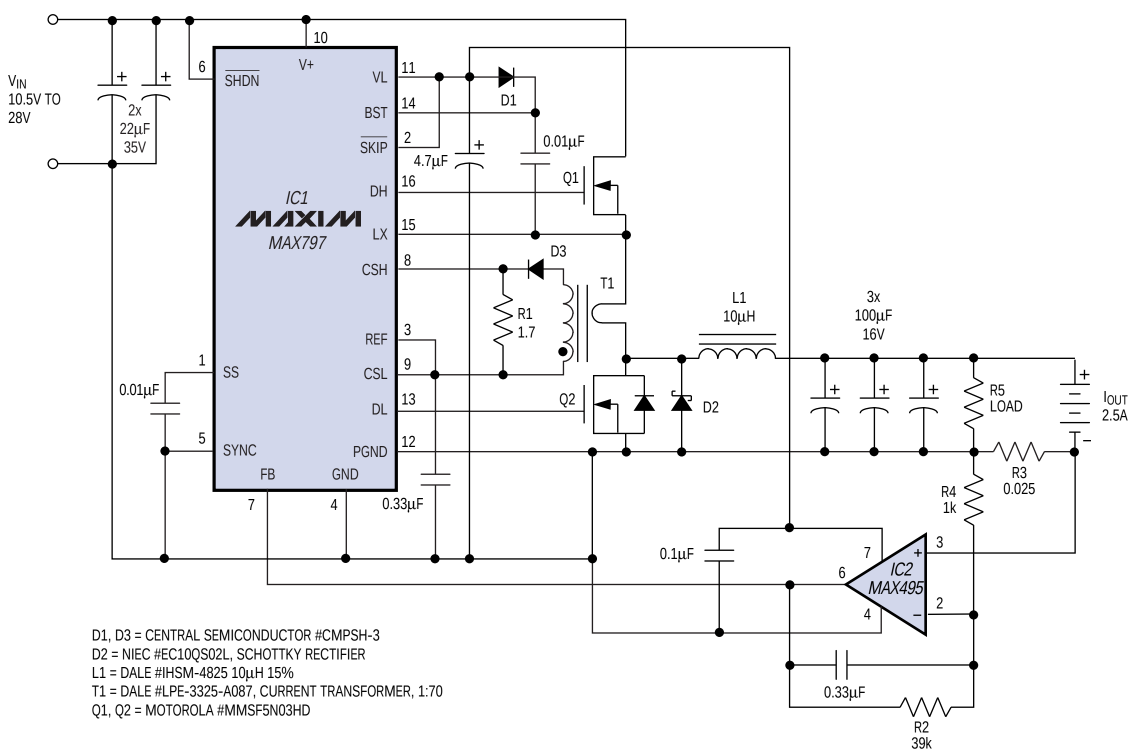


Figure 1. Modified feedback paths transform this switchmode power-supply circuit for notebook computers into a high-efficiency battery charger.

Efficiency exceeds 96% at the higher output voltages (**Figure 2**). (Lower output voltage produces less output power, so the relatively fixed amount of dissipation associated with Q1, Q2, and IC1 represents a larger percentage of the total.) If you inadvertently disconnect the battery during a charge, V_{OUT} cannot rise to a dangerous level (as it can in a boost-mode topology) because the charger's buck-mode topology limits the maximum output voltage to V_{IN}.

A related idea appeared in the 10/12/95 issue of EDN.

(Circle 3)

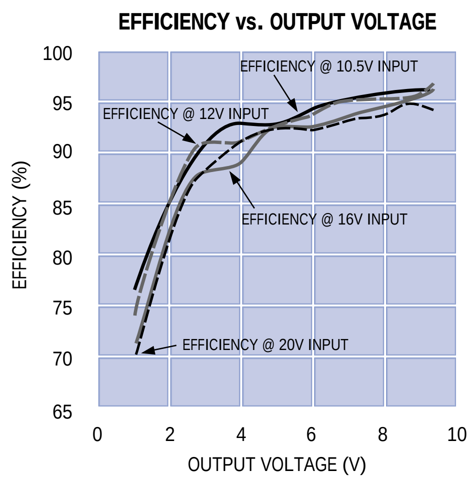


Figure 2. Efficiency for the Figure 1 battery charger rises with output voltage.

DESIGN SHOWCASE

Negative buck regulator employs step-up controller

The circuit of **Figure 1** adopts a step-up (boost) dc-dc controller for use in a negative buck-regulator application. It was developed to power the laser diode in an optical amplifier/booster unit, a job for which no commercial IC was available at the time. The anode of the laser diode connects to ground, so the supply voltage must be negative, and it must deliver 160mA to 750mA.

Although the boost-regulator IC operates in a buck-regulator circuit, its standard connections enable proper control of Q1. The output voltage, however, must be inverted by an op amp for proper voltage feedback: the load is referred to the most positive supply rail instead of IC1's ground terminal, so the controller must increase its duty cycle as V_{OUT} (referred to that terminal) increases. The op amp therefore inverts the feedback signal and shifts it to match the 1.5V threshold internal to IC1.

IC1 is configured in its non-bootstrapped mode, which provides an adequate gate-drive signal (ground to -5.2V) for the external MOSFET Q1. With V_{OUT} set to -3V and the output current ranging from 160mA to above 700mA, the circuit's conversion efficiency ranges from 84% to as high as 87.5% (**Figure 2**).

A related idea appeared in the 11/9/95 issue of EDN.

(Circle 4)

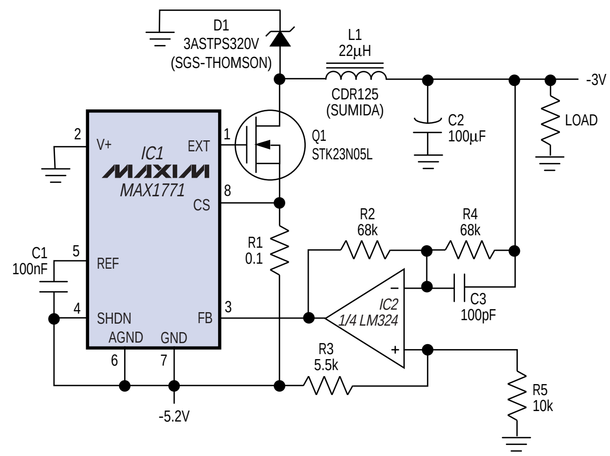


Figure 1. With an external op amp to invert its voltage feedback, this boost-mode dc-dc controller derives a regulated -3V from the -5.2V ECL supply.

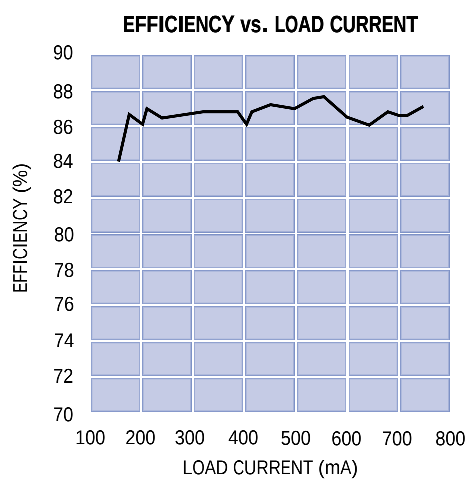


Figure 2. Efficiency for the Figure 1 circuit ranges from 84% to as high as 87.5%.

DESIGN SHOWCASE

5V supply derives power from 3-wire RS-232 port

The circuit of **Figure 1** produces a semi-regulated 5V output from an RS-232 port. Unlike a PC-mouse supply or comparable circuits that rely on the modem-control signals DTR and RTS, this one operates with a 3-wire port (GND, Rx, and Tx), and obtains power only from the Tx line. (Except at high duty cycles, the Tx line, RCV-232, remains operational while supplying power.) The output current—about 8mA—is sufficient for CMOS microcontrollers and other low-power circuits.

IC1 is a switched-capacitor, charge-pump voltage converter that can either invert an input voltage or double it. The connections shown provide a doubler configuration in which the normal input-voltage polarity is reversed: a positive input voltage normally connects between GND and OUT, but this circuit connects a negative input between OUT and GND. The IC then doubles the negative V_{IN} in the positive direction, producing a positive output (at V_{DD}) equal to $|V_{IN}|$.

The zener diode D1 acts as a shunt regulator that "semi-regulates" V_{IN} to -5V (actually to -4.7V). The 33µF capacitor values shown are larger than normal, to support the output voltage during worst-case (all-zero) patterns of transmission. At 9600 baud, for example, an all-zeros character causes an output droop of about 0.2V. For lower baud rates, substitute a proportionally higher value for C1.

A related idea appeared in the 10/26/95 issue of EDN.

(Circle 5)

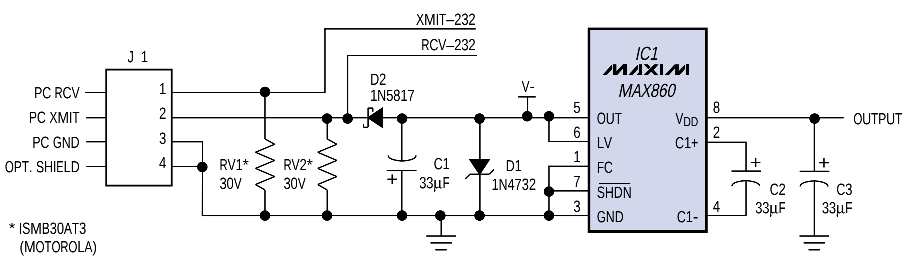


Figure 1. Operating in voltage-doubler mode on a reversed-polarity input voltage, this switched-capacitor voltage converter produces a semi-regulated 5V at 8mA from the Tx line of an RS-232 port.

DESIGN SHOWCASE

Step-up supply charges battery while serving load

The circuit of **Figure 1** supports the many portable applications in which a microprocessor (µP) or microcontroller (µC) controls charging of the battery. IC1 is a step-up switching regulator that boosts V_{IN} (nominally 5V) as necessary to supply the combination of charging current and load current. The 5V source must include short-circuit protection. IC2 is a high-side current-sense amplifier that monitors the charging current. Commands from the processor include CHARGE $\overline{\text{ON}}$/OFF and $\overline{\text{FAST}}$/TRICKLE CHARGE.

IC2 produces an output current (OUT) equal to 10^{-4} of the current through sense resistor R9. Q3 and Q4 are on during a fast-charge operation, so this output current flows through the parallel combination of R11 and (approximately) R4. The resulting feedback to IC1 (pin 3) maintains the fast-charge current through R9 at 500mA. This feedback also enables the regulator to supply as much as 500mA of load current in addition to the fixed 500mA of charging current. Q2 limits the battery voltage to 10V (2V/cell).

During the fast charge, an external processor and multi-channel A/D converter (ADC) must monitor the battery's terminal voltage. When the ADC senses a change of slope in this voltage, the processor terminates the fast charge by asserting a high on $\overline{\text{FAST}}$/TRICKLE CHARGE. Q3 turns off, causing a rise in the feedback (FB) that lowers the charging current to the trickle-charge rate (approximately 60mA).

If IC1 shuts down, or if load current plus charging current exceeds the capability of IC1, the R9 current reverses as current flows out of the battery. IC2 indicates the reversal by allowing R13 to pull its open-collector SIGN output high, turning off Q4 and turning on Q5. Current through R12 then produces a voltage proportional to the battery's discharge current (5A through R9 produces a full-scale response of 3V across R12).

By integrating this voltage over time (sampling at fixed intervals and multiplying by the time interval), the A/D-processor system can monitor energy removed from the battery. Based on this measurement and the terminal-voltage measurement, the processor can then re-initiate a fast charge (by asserting $\overline{\text{FAST}}$/TRICKLE CHARGE low) before the battery reaches its end of life.

A related idea appeared in the 6/8/95 issue of EDN.

(Circle 6)

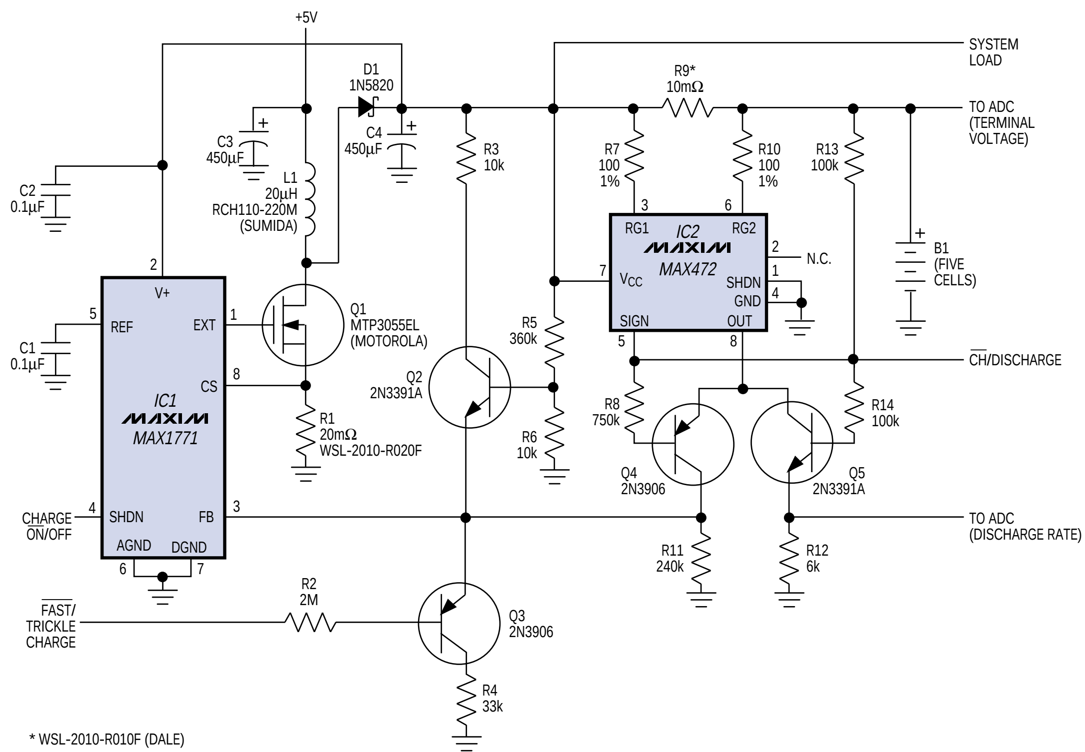


Figure 1. This circuit controls charging of the battery while delivering current to the system load.

NEW PRODUCTS

2.7V, 8-channel, 10- and 12-bit ADCs draw less than 1mA

The 12-bit/10-bit MAX147/MAX148 are 2.7V, low-power data-acquisition systems that include an 8-channel multiplexer, high-bandwidth track/hold, successive-approximation A/D converter, and serial interface. Each monolithic IC is suitable for use in applications that demand minimal power consumption and small size, such as pen-entry devices, hand-held scanners, and portable instruments.

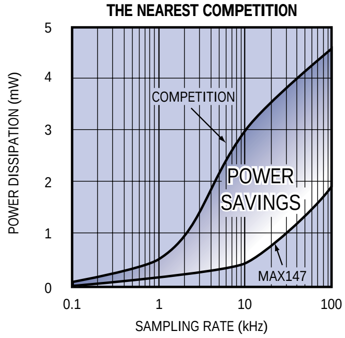
The MAX147/MAX148 supply-voltage range (+2.7V to +5.25V) allows operation in 3V, 3.3V, and 5V systems. Supply current is only 0.9mA at the maximum 133ksps sample rate (V_{DD} = 2.7V), and the 1µA power-down mode minimizes power consumption at all sampling rates. At 10ksps, the average supply current drops to 100µA. This combination of low voltage and low current yields the lowest power dissipation available among comparable converters.

The 4-wire serial-data interface, compatible with SPI™, QSPI™, and Microwire™ standards, enables software configuration for unipolar or bipolar input signals, and for eight single-ended or four differential input channels. A serial-strobe output (SSTRB) allows direct connection to the TMS320 family of digital signal processors.

MAX147/MAX148 devices come in 20-pin DIP and SSOP packages, in versions tested for the commercial (0°C to +70°C), extended-industrial (-40°C to +85°C), and military (-55°C to +125°C) temperature ranges. Prices start at $5.95 for the MAX147 and $4.10 for the MAX148 (1000 up, FOB USA).

(Circle 7)

SAVE POWER OVER THE NEAREST COMPETITION



SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

250MHz, broadcast-quality video op amp has lowest diff. gain/phase: 0.002%/0.002°

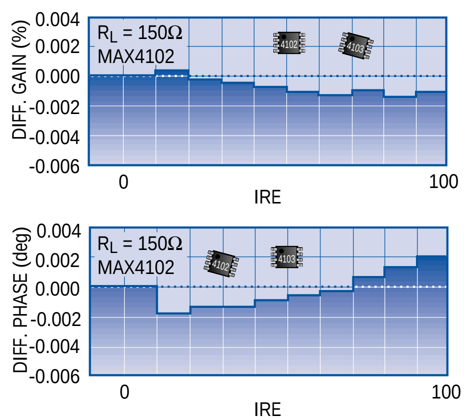
Combining high speed with the lowest differential gain and phase in the industry, the MAX4102/MAX4103 video op amps are suitable for precision applications, such as broadcast and high-definition TV systems, pulse/RF amplifiers, and ADC/DAC amplifiers. Internal compensation provides closed-loop stability for gains of unity and above (MAX4102) or 2V/V and above (MAX4103).

Differential gain and phase errors are 0.002%/0.002° (MAX4102) and 0.008%/0.003° (MAX4103). The MAX4102 delivers a -3dB bandwidth of 250MHz with 0.1dB gain flatness to 130MHz. The MAX4103 delivers a -3dB bandwidth of 1800MHz with 0.1dB gain flatness to 80MHz. Both slew at 350V/µs. Other shared performance includes low distortion (-78dBc SFDR at 5MHz), low-power operation (5mA from ±5V supplies), and 100dB open-loop gain. Each provides an 80mA output-current capability and wide output swings (±3.4V with R_L = 150Ω).

MAX4102/MAX4103 op amps come in 8-pin SO and µMAX packages, screened for the extended-industrial (-40°C to +85°C) temperature range. Prices start at $1.95 (1000 up, FOB USA).

(Circle 8)

Differential Phase & Gain



330MHz closed-loop video buffers offer fixed gains of +1 or +2

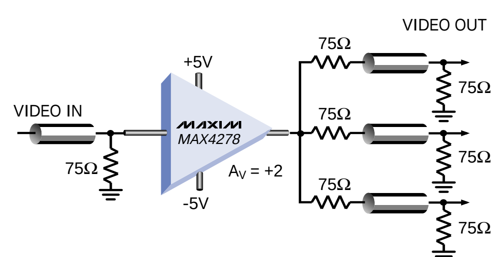
The MAX4178 and MAX4278 closed-loop buffers offer high speed and high output current (100mA). Small-signal bandwidths are 330MHz and 310MHz, respectively, and the slew rates are 1300V/µs and 1600V/µs, respectively. Both buffers exhibit a full-power bandwidth of 210MHz, and 0.1dB gain flatness to 150MHz.

The MAX4178 is preset for a voltage gain of unity (0dB), and the MAX4278 for a voltage gain of 2 (6dB). Both buffers are well suited for driving 50Ω and 75Ω loads. The high slew rates and low power dissipation of these devices are characteristic of current-mode feedback amplifiers, but their unique input stage retains the advantages of voltage-mode feedback as well. The result is low input offset voltage (0.5mV), low input bias current (1µA), and high power-supply rejection (90dB).

Other features include 8mA quiescent supply current, low differential gain/phase errors (0.04%/0.01°), 5nV/√Hz input-referred voltage noise, 2pA/√Hz input-referred current noise, and internal protection against short circuits and ESD (to 8000V).

The MAX4178/MAX4278 buffers come in 8-pin DIP, SO, and µMAX packages, in versions tested for the extended-industrial (-40°C to +85°C) and military (-55°C to +125°C) temperature ranges. Prices start at $2.40 (1000 up, FOB USA).

(Circle 9)



VIDEO DISTRIBUTION AMP

NEW PRODUCTS

Analog muxes and switches operate on low voltage

The MAX4051 8-channel multiplexer, MAX4052 dual 4-channel multiplexer, and MAX4053 triple single-pole/double-throw switch are designed to operate over a wide supply-voltage range: either a single supply of +2V to +16V, or dual supplies of ±2V to ±8V. (The guaranteed limits are +2.7V to +16V, and ±2.7V to ±8V.) Each device offers an A-suffix version that guarantees specified limits for on-resistance match (6Ω), on-resistance flatness (10Ω), and leakage current (0.1nA for on- and off-leakages at +25°C).

Each switch handles rail-to-rail analog signals, and (for 5V or ±5V supplies) the 0.8V and 2.4V digital-input logic thresholds are TTL/CMOS-compatible. MAX4051/MAX4052/MAX4053 devices operating in a 50Ω system measure less than -90dB for crosstalk and off isolation. In 600Ω systems, they offer less than 0.04% signal distortion. In addition, the MAX4051/MAX4052/MAX4053 are pin compatible with the industry-standard ICs 74HC4051, 74HC4052, and 74HC4053.

The MAX4051/MAX4052/MAX4053 and their A-suffix versions all come in 16-pin DIP, QSOP, and narrow-SO packages. Each device is available in versions tested for the commercial (0°C to +70°C), extended-industrial (-40°C to +85°C), and military (-55°C to +125°C) temperature ranges. Prices start at $1.46 (1000 up, FOB USA) .

(Circle 10)

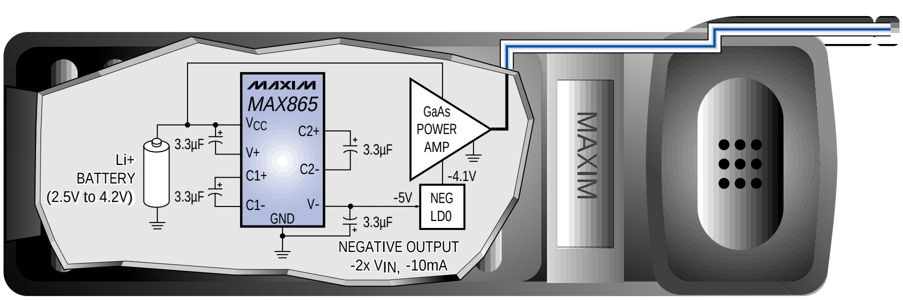
Compact, unregulated charge pump offers bipolar outputs

The MAX865 dc-dc converter includes CMOS charge-pump circuitry that produces unregulated positive and negative outputs from an input voltage between +1.5V and +6V. Available in an ultra-small 8-pin µMAX package, the device is suitable for use as a VCO or GaAsFET supply, as a GaAsFET bias generator in wireless headsets, and as a split supply operating on three Ni cells or one Li+ cell.

The MAX865 requires only four external capacitors. It first doubles the input voltage, then inverts the result to produce a negative output.

To ensure the elimination of switching noise in the audio band, the internal oscillator frequency is guaranteed between 20kHz and 38kHz. Low, 75Ω output impedances allow useful output currents to 20mA. (For logic-controlled shutdown capability and selectable oscillator frequencies, refer to the MAX864.)

The MAX865's 1.11mm-high µMAX package occupies half the board area of a standard 8-pin SOIC, and is screened for the extended-industrial (-40°C to +85°C) temperature range. Prices start at $1.30 (1000 up, FOB USA).



Smallest 25mA charge pumps fit in SOT23-5 package

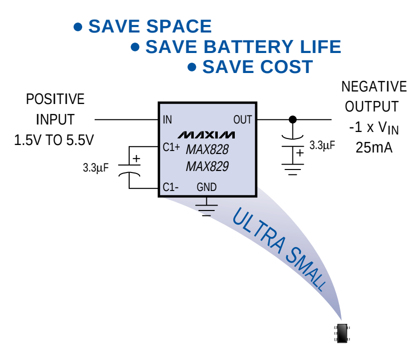
The MAX828/MAX829 are the world's smallest inverting charge pumps. Available in 5-pin SOT23-5 packages, these 25mA-output dc-dc converters convert positive voltages to negative voltages for use in cellular telephones, LCDs, data-acquisition systems, and analog-signal measurement systems. The ultra-small SOT23-5 package occupies just $0.013in^2$ ($8.4mm^2$) and is just 1.45mm high.

MAX828/MAX829 devices require only two small external capacitors to form a complete circuit. Their 20Ω typical output resistance permits useful output currents to 25mA. The input voltage range is +1.5V to +5V.

The MAX828 targets applications in which low power consumption is most critical. It switches at 12kHz, requires 10µF capacitors, and draws only 90µA of quiescent current. The MAX829 targets applications for which space is critical. It draws 150µA supply currents and switches at a higher frequency (35kHz), which enables the use of smaller, 3.3µF capacitors. Because its 35kHz switching frequency is above the 20kHz audio range, the MAX829 also targets low-noise audio applications.

MAX828/MAX829 charge pumps come in SOT23-5 packages screened for the extended-industrial temperature range (-40°C to +85°C). Prices start at $1.30 (2500 up, FOB USA).

(Circle 12)



NEW PRODUCTS

High-efficiency step-down controllers offer 5V, 3.3V, or adjustable outputs

The MAX1626/MAX1627 step-down dc-dc switching controllers offer high efficiency for load currents ranging from 1mA to more than 2A. Their current-limited, pulse-frequency-modulated (PFM) control scheme operates with duty cycles to 100%, resulting in very low dropout voltages. This unique control scheme also eliminates minimum-load requirements, and lowers the light-load supply current to 90µA—vs. 2mA to 10mA for common pulse-width-modulation (PWM) controllers.

Each MAX1626/MAX1627 controller drives an external p-channel MOSFET, allowing design flexibility for applications of 12.5W and higher. Soft-start capability reduces the current surges that otherwise occur at start-up. High switching frequencies (to 300kHz) and a "continuous-conduction" mode of operation enable the use of tiny surface-mount inductors, which minimizes system cost and pc-board area.

Input voltages can range from +3.0V to +16.5V. The MAX1626 offers preset outputs of 5V and 3.3V, and the MAX1627 offers an adjustable output voltage. Quiescent currents (90µA maximum) drop to 1µA maximum in shutdown mode. The MAX1626/MAX1627 are functional upgrades for the MAX1649/MAX1651.

The MAX1626/MAX1627 come in 8-pin SO packages, screened for the extended-industrial temperature range (-40°C to +85°C).

(Circle 13)

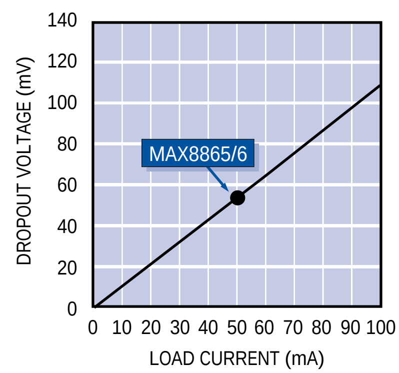
Dual linear regulator delivers 50mA with 55mV dropout

The MAX8865/MAX8866 dual linear regulators operate from input voltages of +2.5V to +5.5V and deliver as much as 100mA per output. Their tiny µMAX package and low supply current (only 105µA) make them ideal for use in battery-operated portable equipment, such as cellular phones, cordless phones, and modems.

Each device features Dual Mode™ operation: its output voltage is either preset (3.15V for T-suffix versions, 2.84V for S-suffix versions, or 2.80V for R-suffix versions) or adjustable via an external resistor divider. Other features include low-power shutdown and protection against short circuits, overheating, and reversed batteries. The MAX8866 also includes auto-discharge circuitry, which, in shutdown mode, actively crowbars the selected output voltage to ground.

MAX8865/MAX8866 regulators are available in 8-pin µMAX packages, screened for the extended-industrial temperature range (-40°C to +85°C). Prices start at $1.46 (1000 up, FOB USA).

(Circle 14)



Dual Mode is a trademark of Maxim Integrated Products.

8-pin µP supervisors with battery backup now available in µMAX packages

MAX817/MAX818/MAX819 microprocessor (µP) supervisors require only 11µA of supply current, yet combine all the standard µP-supervisory functions—including battery backup—in an 8-pin µMAX package.

Intended for use with 5V supplies, the devices come in two supply-threshold versions: the L-suffix versions, intended for ±5% supplies, have 4.65V thresholds; and the M-suffix versions, intended for ±10% supplies, have 4.40V thresholds. All are designed to ignore fast transients on V_{CC}.

The three ICs differ according to the features and supervisory functions they offer (see Table). These include active-low resets, backup-battery switchover, chip-enable gating, watchdog input (for monitoring software execution), and battery-freshness seal (disconnects the backup battery when not in use). The chip-enable propagation delay (8ns maximum) is the lowest in the industry.

These supervisors come in 8-pin DIP, SO, and µMAX packages, in versions tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges. Prices start at $2.44 for the MAX817, $2.74 for the MAX818, and $2.07 for the MAX819 (1000 up, FOB USA).

(Circle 15)

FEATURE	MAX817L/M	MAX818L/M	MAX819L/M
Active-Low Reset	✔	✔	✔
Backup-Battery Switchover	✔	✔	✔
Power-Fail Comparator	✔	–	✔
Watchdog Input	✔	✔	–
Battery Freshness Seal	✔	✔	✔
Manual Reset Input	–	–	✔
Chip-Enable Gating	–	✔	–
Pins-Package	8-DIP/SO/µMAX	8-DIP/SO/µMAX	8-DIP/SO/µMAX
Lower Power Pin-Compatible Upgrade for:	MAX690A/692A	MAX691A/693A (functional equivalent)	MAX703/704

NEW PRODUCTS

World's first 1-Rx/1-Tx RS-232 transceiver draws only 1µA supply current

The MAX3221 transceiver provides a 3V-powered, EIA/TIA-232 and V.28/V.24 communications interface for notebook computers and other portable applications. It combines a proprietary, high-efficiency dual charge pump and a low-dropout transmitter to deliver true RS-232 performance from a single power supply of +3.0V to +5.5V. The guaranteed data rate (120kbps) ensures compatibility with software currently popular for personal-computer communications.

The MAX3221 saves power with Maxim's patented AutoShutdown™ feature. If the RS-232 cable is disconnected or if the remote transmitters are shut down, AutoShutdown™ senses, within 30µs, the consequent absence of valid signal levels at the receiver inputs. The transceiver then shuts down its drivers and its charge-pump power supply, reducing the quiescent supply current to 1µA. A valid signal level at any receiver input wakes up the transceiver automatically. The resulting power savings are achieved without modification to the existing BIOS or operating system.

A low-dropout output stage enables the MAX3221 to operate with an internal voltage doubler in place of the tripler required by other transceivers. The doubler requires only four external capacitors, rather than the five required by a tripler. It also saves power during data transmissions, delivering 50% greater efficiency than a tripler.

The MAX3221 requires only four external 0.1µF capacitors for 3.3V operation. The transceiver is suitable for 3.3V-only systems, mixed 3.3V and 5V systems, and 5V-only systems that require true RS-232 performance. It offers a 6V/µs minimum-guaranteed slew rate, and meets EIA/TIA-232 specifications for supply voltages as low as +2.7V.

The MAX3221 comes in a 16-pin SSOP package, in versions tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges. Prices start at $1.25 (1000 up, FOB USA).

(Circle 16)

AutoShutdown is a trademark of Maxim Integrated Products.

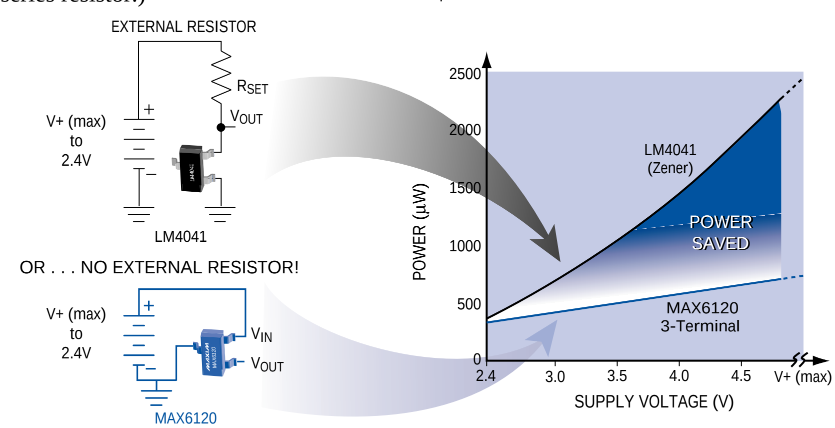
First three-terminal precision reference in a SOT23-3 package

The MAX6120 is the first micropower, three-terminal, 1.2V precision voltage reference available in a SOT23-3 package. Ideal for 3V battery-powered equipment in which power conservation is critical, the MAX6120 offers a low-power alternative to existing two-terminal shunt references. (Two-terminal references draw excessive battery current and require an external series resistor.)

The MAX6120's 50µA supply current is independent of input voltage over temperature, so the device offers maximum efficiency at all battery voltages. For SOT23-3 packages, the initial accuracy is ±1% and the temperature coefficient of output voltage is only 30ppm/°C (100ppm/°C maximum).

MAX6120 references come in 8-pin SO and 3-pin SOT23-3 packages, screened for the extended-industrial (-40°C to +85°C) temperature range. Prices start at $0.80 (1000 up, FOB USA).

(Circle 17)



3.3V data interface provides line isolation for RS-485 systems

The MAX3480A/MAX3480B data interface provides 3.3V operation and complete galvanic isolation for half-duplex (party-line) RS-485 communications systems. Each device includes transceivers, optocouplers, and a transformer in a single low-cost, 28-pin DIP. MAX3480A drivers allow transmission rates to 2.5Mbps. The MAX3480B's slew-rate-limited drivers minimize EMI, reduce reflections caused by improperly terminated cables, and enable error-free transmissions to 250kbps.

A single 3.3V supply on the logic side of each device provides power to both sides of the isolation barrier. (For 5V systems, consider the MAX1480 and MAX1490.) Typically, the MAX3480A/ MAX3480B barrier can withstand as much as 1600V_{RMS} for one minute or 2000V_{RMS} for one second. Typical quiescent supply current is 180mA, and the MAX3480B has a low-power shutdown mode that lowers this current to 0.2µA.

The driver outputs are short-circuit current limited, and include thermal-shutdown circuitry that places the outputs in a high-impedance state to guard against excessive power dissipation. As a fail-safe feature, each receiver guarantees a logic-high output when its input is open circuited.

MAX3480A/MAX3480B devices come in 28-pin plastic DIPs, in versions tested for the commercial (0°C to +70°C) and extended-industrial (-40°C to +85°C) temperature ranges. Prices start at $15.76 for the MAX3480A and $14.95 for the MAX3480B (1000 up, FOB USA).

(Circle 18)